Shallow Trench Isolation Void Detecting Method and Structure for the Same

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention relates to a semiconductor device process, more specifically, to a method for detecting if there is any void in STI.

2. Description of the Prior Art

In the process for semiconductor devices getting more and more compact, shallow trench isolation (STI) is used to separate active areas 10 for forming respective elements. STI is formed between active areas 10 and is filled with dielectric 12, which can be oxide such as silicon oxide. However, a void 13 is likely to be generated in the step of filling with the dielectric 12, as shown in Fig. 1.

In DRAM process, such a condition also happens. With reference to Fig. 2, which is a schematic top view of a gate region structure of a DRAM, reference number 20 indicates an active area, 21 indicates a gate line, 24 indicates a deep trench. As shown in the drawing, the adjacent portion between the active areas is short. Reference number 23 indicates a void formed in the dielectric filled in the STI between the active areas 20. The existence of the void 23 may influence the electric performance of the semiconductor structure. However, such a void is very small and is hardly found during the process. Usually, the existence of the void only can be found in the electric testing, which is performed after the wafer is finished, cut into chips and packed. Accordingly, a waste of process is generated.

Therefore, there is a need for a solution to overcome the problems stated above. The present invention satisfies such a need.

SUMMARY OF THE INVENTION

An objective of the present invention is to provide a STI void detecting method for semiconductor wafers. The method of the present invention can find in time whether there is any void formed in STI, so that the defective products can be found in the early stage, thereby reducing the waste of the cost and working hours.

Another objective of the present invention is to provide a STI void detecting region

structure for semiconductor wafers. By forming and testing the testing region structure of the present invention, whether there is any void formed in STI can be found in time.

According to an aspect of the present invention, a shallow trench isolation void detecting method for a semiconductor wafer comprises steps of assigning a testing region in a predetermined region of the semiconductor wafer; forming active areas and gate lines inter with the active areas in said detecting region by a synchronous process for other regions, filling a trench between the active areas with dielectric, the adjacent portion between the active areas having at least a predetermined length; and detecting the electric values of the gate lines to determine whether there is a void formed in the dielectric filled in the trench between the active areas.

According to another aspect of the present invention, a testing region structure for semiconductor wafer STI void detecting is formed on the wafer by a process synchronizing for other portions of the wafer. The testing region structure comprises a plurality of active areas, trenches between the active areas being filled with dielectric, and the portions of the active areas adjacent to each other having at least a predetermined length; and a plurality of gate lines inter with the active areas.

BRIEF DESCRIPTION OF THE DRAWINGS

The following drawings are only for illustrating the mutual relationships between the respective portions and are not drawn according to practical dimensions and ratios. In addition, the like reference numbers indicate the similar elements.

Fig. 1 shows a schematic sectional diagram illustrating a void formed in a STI of a semiconductor device;

Fig. 2 is a schematic top view showing the arrangement of the active areas and gate lines of a semiconductor device in prior art; and

Fig. 3 is a schematic top view showing the arrangement of the active areas and gate lines of a semiconductor device in accordance with an embodiment of the present invention.

DETIALED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will be described in detail with reference to the accompanying drawings.

According to an embodiment of the present invention, at predetermined locations on the wafer, preferably the cut lines portion, testing regions comprising active areas and gate lines

are produced by the synchronous process for other portions of the wafer.

As shown in Fig. 3, the sections of active areas 30 in the testing region are formed as long strips. Accordingly, the active areas 30 are adjacent to each other. Shallow trenches formed between the active areas 30 are filled with dielectric 32 by the process synchronous with other portions of the wafer. As shown, in the present embodiment, the active areas 30 are preferably formed as parallel strips. Since the length of the portions of two active areas 30 adjacent to each other is very long, if there is a void 33 formed in the dielectric 32, the void 33 will be a long void. Gate lines 31' in the testing region are arranged at an interval the same as the gate lines in other non-testing regions. As shown, since the section of the void 33 is long, the void 33 crosses at least two gate lines 31'. Accordingly, for example, it is easy to detect whether there is a void existing by measuring the potentials of the gate lines 31' in the testing region.

According to the present embodiment, for the sake of convenience of measuring, the gate 31 can be formed as a comb-shaped gate. That is, the odd gate lines connected together, while the even gate lines connected together, thereby forming a dual-comb structure. Then the potential of a plurality of gate lines can be measured at a time.

The testing region is produced synchronously with other regions of the wafer. Accordingly, if a void is detected in the testing region, it can be determined that there are voids formed in other portions of the wafer. Then the detective products can be found and eliminated at an early stage, but not the stage after the wafer is cut into chips and packed. Thus, unnecessary working process is avoided, and therefore the working hours and cost are reduced.

While the embodiment of the present invention is illustrated and described, various modifications and alterations can be made by persons skilled in this art. The embodiment of the present invention is therefore described in an illustrative but not restrictive sense. It is intended that the present invention may not be limited to the particular forms as illustrated, and that all modifications and alterations which maintain the spirit and realm of the present invention are within the scope as defined in the appended claims.